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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,870	08/27/2001	Yoko Hayashida	N26180400W	4837

7590 08/22/2003

Darryl G. Walker  
WALKER & SAKO, LLP  
Suite 235  
300 South First Street  
San Jose, CA 95113

EXAMINER

NGUYEN, DANNY

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 08/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/939,870

Applicant(s)

HAYASHIDA ET AL. *cu*

Examiner

Danny Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 June 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-20 is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-8, 12-15 is/are rejected.
- 7) ☒ Claim(s) 4 and 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \*   c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-3, 7, 8, 10, 12, 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Tailliet (USPN 5,515,226).

Regarding to claims 1, 3, 15, APA discloses that an apparatus for a semiconductor integrated circuit device (see fig. 17) comprises a plurality of transistors (112a to 112c) coupled to a corresponding I/O terminal (110a to 110c) through a corresponding first resistance (R114a to R114c); a first clamping device (111a) coupled to each I/O terminal (110a); a second clamping circuit (113a to 113c) corresponding to each transistor, each second clamping circuit including a second clamping device (113a) and the corresponding the first resistance, each second clamping device having a first terminal connected to the gate of the corresponding transistor (112a to 112c) and a second terminal connected to a source/drain of the corresponding transistor and a supply potential wiring (117); each first clamping device being coupled to one second clamping device through a second resistance (wiring resistance 117). APA does not disclose that at least two of the second clamping devices are different. Tailliet discloses that a second limiter (EC2j) of semiconductor integrated circuit device (fig. 3) can be varied depending on the location of the transistor. Tailliet discloses the second limiter

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(EC2j) of transistor (ELj) can be varied depending on the protection level needed by the transistor (ELj) due to its location relative to the pad which it is connected to (see col. 3, lines 15-19). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to utilize the teaching of Tailliet in order to vary the second clamping circuit of APA in order to provide the protection as needed by the individual transistor depending on its location and protection level needed.

Regarding to claim 2, APA discloses that a supply potential wiring is selected from the group of consisting of an electric power supply potential wiring (118), and a ground electric potential wiring, and a substrate electric potential wiring (117) (see p. 3, lines 2-3).

2. Claims 5 and 6, the APA in view of Tailliet disclose all limitations of claim 1. APA and Tailliet do not disclose that a length of wiring connects the second clamping devices (113a) to the gate and the drain/source of the corresponding transistor (112a) is no more than 100 micrometers. However, it would have been obvious to one having ordinary skill in the art at the time invention was made to substitute a length of wiring to any desired values as long as it is compatible with the requirements of the other components in the integrated circuit in order to minimize any resistance between its components. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding to claim 7, APA discloses that the first resistance (R114) comprises a wiring resistance and contact resistance (see fig. 15).

Regarding to claim 8, APA discloses that the first resistance includes a non-wiring structure (internal resistor 114).

Regarding to claim 10, APA discloses that the second resistance (114a) comprises a supply potential wiring (118) and a contact resistance where the first and second clamping devices are connected to the supply potential wiring (118) (see fig. 18).

Regarding to claims 12 and 13, APA does not disclose that each first clamping device (111a) and each second clamping device connected to a different supply terminal. Tailliet discloses the first clamping circuit (EC1j) and second clamping circuit (EC2j) are connected to different power supply terminal (between Pj and P1, see fig. 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to utilize the teaching of Tailliet in order to vary the second clamping circuit of APA in order to provide the protection as needed by the individual transistor depending on its location and protected level needed.

3. Claim 14, APA in view of Tailliet disclose all limitations of claim 1 except for each second clamping device selected from a group as claimed. As for the clamping device being various elements (an IGFET, an NPN bipolar, a diode, and a thyristor); it would have been obvious to one of ordinary skill in the art at the time the invention was made to select any known over-voltage protection element as deemed suitable in order to provide the over-voltage protection function. This is further demonstrated by applicant's various embodiments of the over-voltage protection as claimed absent persuasive evidence that particular type of over-voltage protection element is significant.

***Allowable Subject Matter***

4. Claims 16-20 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 16 recites a method for designing a CDM model protective circuit for a semiconductor circuit comprises step of selecting a ratio of the second resistance and the first resistance that prevents potential between the gate and the source terminal of the first IGFET from exceeding a threshold value.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such limitation.

5. Claims 4, and 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 recites a CDM model protective circuit for a semiconductor circuit comprises a ratio of the second resistance and the first resistance that prevents potential between the gate and the source terminal of the first IGFET from exceeding a threshold value.

Claim 9 recites a CDM model protective circuit for a semiconductor circuit comprises at least one first resistance including an effective channel resistance of an input path IGFET.

Claims 10, 11 recite a CDM model protective circuit for a semiconductor circuit comprises the second resistance which comprises essentially a contact resistance

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between the second terminal of the first clamping device and the supply potential wiring, a supply potential wiring between the first clamping device and the supply terminal, a supply terminal resistance, a supply potential wiring between the supply terminal and the second terminal of the second clamping device, a contact resistance between the second terminal of the second clamping device and supply potential wiring.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such limitation.

### ***Response to Arguments***

6. Applicant's arguments filed 6/17/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., CDM model) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding to claims 1-3, 5-7, 10, 11, 13-15, applicant argued that the Tailliet reference is not related to a CDM model, but this argument is not shown in claim 1. In addition, applicant also argued that the Tailliet reference does not show variation two second limiters, However, Tailliet teaches plurality of second voltage limiters vary from each other by the internal resistor ( $R_j$ )(see col. 4, lines 34-47). Thus applicant's arguments of claim 1 do not overcome the Tailliet reference.

Regarding to claim 12, applicant argued that P1 is not a power supply terminal. Tailliet discloses P1 is a power supply terminal (col. 1, lines 52-53). Therefore, applicant's arguments of claim 12 are not persuasive.

Regarding to claim 8, applicant argued that the limitations of claim 8 are not addressed. However, these limitations are addressed in the rejections sent on 10/07/2002. Therefore, applicant's arguments of claim 8 are not persuasive.

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers



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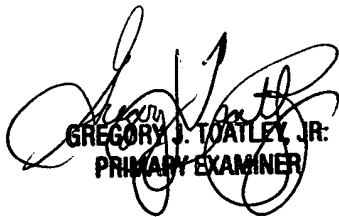
for the organization where this application or proceeding is assigned are (703)-872-9318 for regular communications and (703)-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

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August 15, 2003

  
GREGORY J. TOATLEY, JR.  
PRIMARY EXAMINER